Academic Year 2023 - 2024

Question Bank

Year/Semester: II/III	Department :ECE	Unit : I/II/III/IV/V
Date: **13/ 1** /2024	Subject Code/Title :EC3352 Digital system design	Section : Part A/B/C
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UNIT- I BASIC CONCEPTS

PART-A

1. State De Morgan's theorem. (or) State De Morgan's Law and write any one application.

De Morgan suggested two theorems that form important part of Boolean algebra. They are,

1) The complement of a product is equal to the sum of the complements.

$(AB)' = A' + B'$

2) The complement of a sum term is equal to the product of the complements. $(A + B)' = A'B'$

Application: useful in the implementation of the basic gate operations with alternative gates.

2. Sketch the waveform of each inverter output in the given diagram.
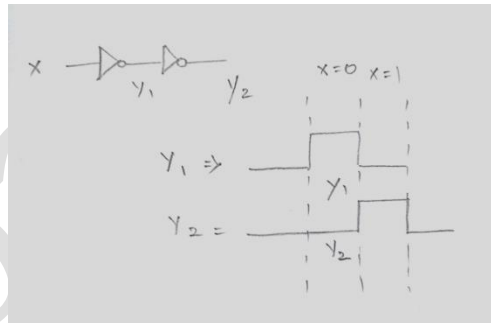
3. What is meant by maxterm and true max term ?

Each and Individual term in standard POS form is called as maxterm.
Maxterm (standard sum term) A sum (OR) of n Boolean variables, uncomplemented or complemented but not repeated, in a Boolean function of n variables.

4. What is the basic priciple used in order to check or generate the proper parity bit in a given code word?

Parity bit is defined as the addition of extra bit in order to make as a odd or even parity for detecting the errors in the codes.
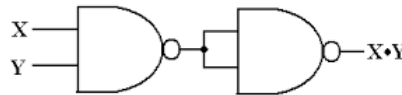
5. Convert the given decimal numbers to their binary equivalent 108.364, 268.025
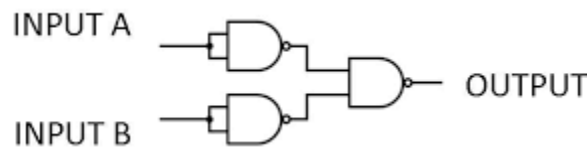
108.364 = 01101100   268.025 = 0000000100001100

6. Show how to connect NAND gate to get AND and OR gate?

AND using NAND

OR using NAND

7. Simplify the following expression X.Y +X(Y+Z)+Y(Y+Z).

$$X.Y + X(Y+Z) + Y(Y+Z) = XY + XY + XZ + Y + YZ$$
$$= X(Y+Z) + Y(1+YZ)$$

8. Why totem pole outputs cannot be connected together?
   Totem pole outputs cannot be connected together because such a connection might produce excessive current and may result in damage to the devices

9. Prove that Boolean theorems.
   (a) $x + x = x$
        $= x + x$
        $= x$
   (b) $x + xy = x$
        $= x(1+y)$
        $= x$

10. Define noise margin.
   Noise margin is the amount by which a signal exceeds the minimum amount for proper operation. In a digital circuit, the noise margin is the amount by which the signal exceeds the threshold for a proper '0' or '1'.

11. Express the function Y=A+B'C in a Cannonical POS.

Y= A+B'C = A(B+B')(C+C') + B'C(A+A')

            = ABC + ABC'+AB'C + AB'C' + AB'C + A'B'C

            = ABC + AB'C + ABC' +AB'C' + A'B'C

12. Convert Y = A+BC'+AB+A'BC

          Y= A(B+B')(C+C')+ AB(C+C')+A'BC

        = AB+AB'(C+C') + ABC+ABC'+A'BC

        = ABC+ABC'+AB'C+AB'C'+ABC+ABC'+A'BC

        =ABC+ABC'AB'C+AB'C'+A'BC

13. Simplify the following Boolean expression into one literal W'X(Z'+YZ)+X(W+Y'Z).

      W'X(Z' + Y'Z) + X(W + W'YZ) to 1 literals

      = W'XZ' + W'XY'Z + WX + W'XYZ

      = WX + W'XZ' + W'XZ = WX + W'X = X

14. Convert 0.35 to equivalent hexadecimal number.

      Decimal 0.35 = Hexadecimal 0.599

15. State distributive law.

      The distributive property states that AND ing several variables and OR ing the result with a single variable is equivalent to OR ing the single variable with each of the the several variables and then AND ing the sums. The distributive property is:

A+BC= (A+B) (A+C)

      A.(B+C)= (A.B) + (A.C)

16. What is a prime implicant?

      A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map.

17. What are called don't care conditions?

      In some logic circuits certain input conditions never occur, therefore the corresponding output never appears. In such cases the output level is not defined, it can be either high or low. These output levels are indicated by 'X' or'd' in the truth tables and are called don't care conditions or incompletely specified functions.

18. Simplify the given Boolean expression F=x'+xy+xz'+xy'z'.

      X'Y' + Y'Z + XZ + XY + YZ' = X'Y' + XZ + YZ'

      = X' Y' + Y' Z(X + X') + XZ + XY + Y Z'

      = X' Y' + X Y' Z + X' Y' Z + XZ + XY + Y Z'

      = X' Y' (1 + Z) + X Y' Z +XZ + XY + Y Z'

      = X' Y' + XZ(1 + Y') + XY + Y Z'

      = X' Y' + XZ + XY (Z + Z')+ Y Z'

      = X' Y' + XZ + XY Z +Y Z' (1 + X)

      = X' Y' + XZ(1 + Y) + Y Z' = X' Y' + XZ + Y Z'

19. Which gates are called as the universal gates? What are its advantages?

   The NAND and NOR gates are called as the universal gates. These gates are used to perform any type of logic application.

20. What is propagation delay?

   Propagation delay is the average transition delay time for the signal to propagate from input to output when the signals change in value. It is expressed in ns.

PART-B

1. Minimize the following expression : using tabulation method.

   $f = \sum m\ (\ 0,1,2,8,9,15,17,21,24,25,27,31)$

2. A stair case light is controlled by two switches, one is at the top of the stairs and other at the bottom of the stairs :

   i) Make a truth table for the system

   ii) Write the logic equation in the SOP form

   iii) Realize the circuit using AOI logic

   iv) Realize the circuit using minimum number of   a) NAND Gates   b) NOR Gates

3. i) Simplify the Boolean expression using laws and rules of Boolean algebra

   $Z = [\ AB'\ (C+BD) + (AB')].C.$

   ii) Define SOP and POS term. Convert the Boolean expression

   AB'C + B'CD+AC,D to SOP form.

4. i) Implement the Boolean expression using minimum number of 3 input NAND gate

   $f(A,B,C,D) = \sum (1,2,3,4,7,89,10,12$

5. (i) State and prove De morgan's theorem

   (ii) Find a MinSOP and MinPOS for

   F=b'c'd+acd'+a'b'c+a'bc'd.

6. (i) Find the MSOP representation for F(A,B,C,D,E) = m(1,4,6,10,20,22,24,26)+d(0,11,16,27) using K-map method. Draw the circuit of the minimal expression using only NAND gates.

   (ii) With neat circuit diagram, explain the function of 3-input TTL NAND gates.

7. What are the advantages of using tabulation method? Determine the minimal sum of products for the Boolean expression $F = \sum (1,2,3,7,8,9,10,11,14,15)$ using tabulation method.

8. Simplify the following Boolean function by using Quine- Mccluskey method and verify the result using K-map $F(\ A,\ B,\ C\ ,\ D\ ) = \sum (0,\ 2,\ 3,\ 5,\ 7,\ 9,\ 11,\ 13,\ 14$

9. (i) Draw and explain Tri-state TTL inverter circuit diagram with its operation.

   (ii) Implement the following function using NAND and inverter gates.

   $F = AB + A'B' + B'C.$

10. (i) Minimize the following logic function using K-maps and realize using NAND and NOR gates. $F(A,B,C,D) = \sum m(1,3,5,8,9,11,15)+d(2,13)$

   (ii) Show that if all the gate in a two-level OR-AND gate network are replaced by NOR gate, the output function does not change.

11. (i) Realize NOT, OR, AND gates using universal gates.

   (ii) Discuss about the basic operation of TTL NAND gate.

12. (i) Simplify T(x,y,z) = (x+y)[(x'(y'+z'))']+x'y'+x'z'.

   (ii) Simplify the following Boolean function and draw the logic diagram

     f(w,x,y,z) = $\sum$(0,1,2,4,5,6,8,9,12,13,14).

13. Simplify the given Boolean function using tabulation method

    F(A,B,C,D,E)=$\sum$ m (0,1,4,5,16,17,21,25,29).

14. (i) Convert the following function into Product of Maxterms

    F(A,B,C) = (A+B')(B+C)(A+C').

   (ii) Using QuineMcClusky method, simplify the given function.

    F(A,B,C,D)= $\sum$m(0,2,3,5,7,9,11,13,14).

15. (i) Draw the multi level two input NAND circuit for the following expression: F=(AB'+CD')E + BC(A+B).

   (ii) Draw & explain Tri-state TTL inverter circuit diagram & explain its operation.


PART-C

1. (i) Given Y(A,B,C,D) = $\sum$ m(0,1,3,5,6,7,10,14,15) draw the K-map and obtain the simplified

    expression. Realize the minimum expression using basic gates.

   (ii) Implement the expression Y(A,B,C) = $\sum$ m(0,2,4,5,6) using only NOR-NOR logic.

   (iii) Implement EXOR gate using only NAND gates.

2. Simplify the following function using tabulation method

  Y(A,B,C,D)= $\sum$ m (0,1,2,5,6,7,8,9,10,14) and implement using only NAND gates.

3. (i) Simplify xy+x'z+yz.

   (ii) Simplify the following expression using K-map method.

    Y= $\sum$ m(7,9,10,11,12,13,14,15).

4. (i) Write short notes on don't care conditions.

   (ii) Explain about NAND and NOR implementations.

5. Minimize the given switching function using Quine-Mccluskey method.

    F(x_1,x_2,x_3,x_4) = $\sum$(0,5,7,8,9,10,11,14,15).

UNIT - II COMBINATIONAL LOGIC CIRCUIT
PART-A

1.Draw the logic diagram of 4bit parallel subtractor. (A/M 18)
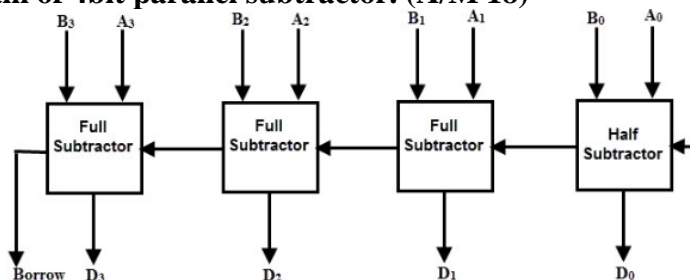
**2. Draw the full adder circuit using half adder. (N/D 17)**
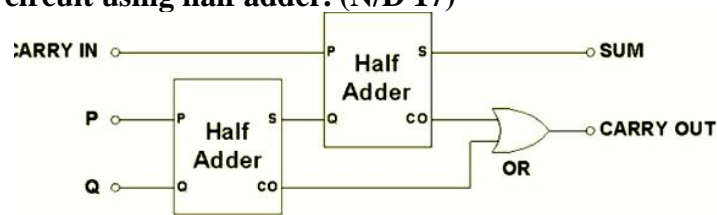
3. Write the function of magnitude comparator. (N/D 17)

Magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number.
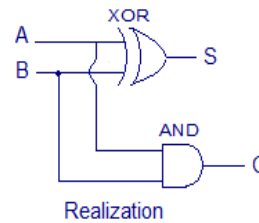
4. Draw the truth table and the logic circuit of half adder. (A/M17)

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Truth table
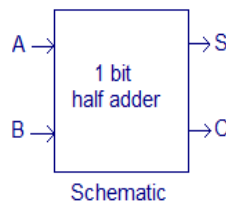
5. Compare the function of decoder and encoder. (A/M17)

Encoder: An encoder is a digital circuit that performs the inverse operation of a decoder.
An encoder has 2^n input lines and n output lines.

Decoder: A decoder is a multiple-input, multiple-output logic circuit which converts coded inputs into coded outputs, where the input and output codes are different.

6. Write about the design procedure for combinational circuits. (N/D 16, M/J 16)

- The problem definition
- Determine the number of available input variables & required O/P variables. Assigning letter symbols to I/O variables
- Obtain simplified Boolean expression for each O/P.
- Obtain the logic diagram.

7. Draw the logic diagram and truth table of full adder. (N/D 16)
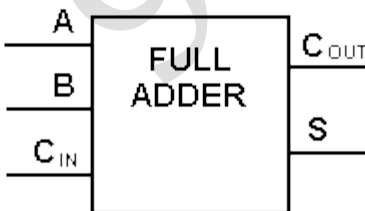
Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Logic diagram and truth table of full adder.

8. Draw the combinational circuit that converts 2 coded inputs into 4 coded outputs. (M/J 16)
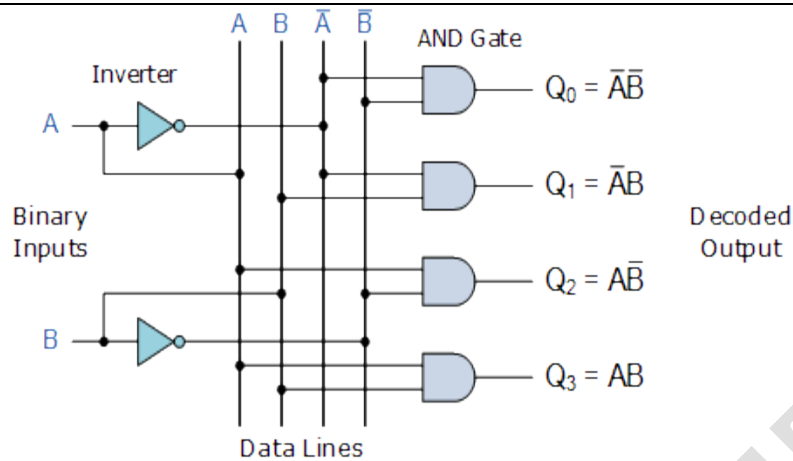
9. Define Half adder and full adder. (N/D 15, M/J 13)

The logic circuit that performs the addition of two bits is a half adder. The circuit that performs the addition of three bits is a full adder.

10. What is priority Encoder? (N/D 15, M/J 14)

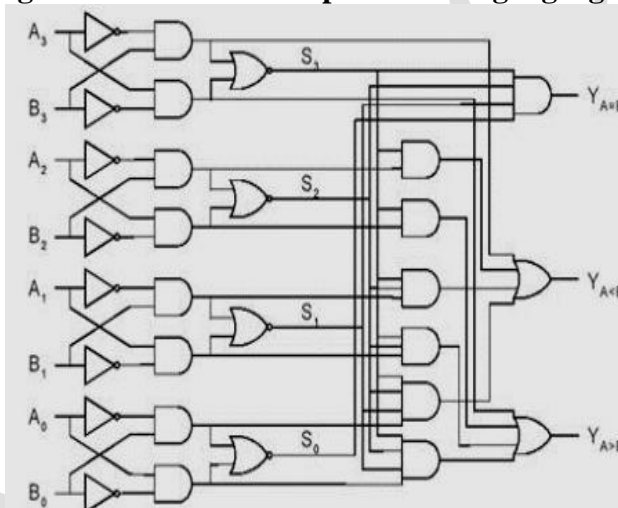A priority encoder is an encoder circuit that includes the priority function. In priorityencoder, if 2 or more inputs are equal to 1 at the same time, the input having the highestpriority will take precedence.

11. Draw the logic circuit of 2 bit comparator using logic gates. (A/M 15, M/J 14)

12. Write down the difference between demultiplexer and decoder.(A/M 15)

A demux simply selects an output line, nothing more. It's a glorified switch. A decoder takes n inputs, and uses those inputs to determine which of the 2^n output lines is high.
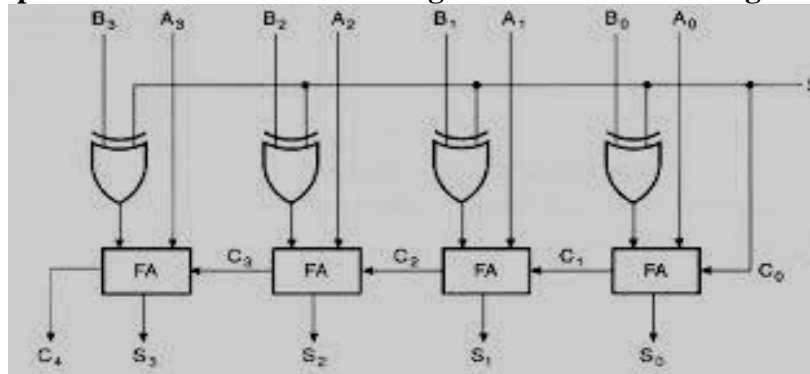
13. Give the logic expression for the sum and carry in full adder circuit. (A/M 15)

1. Sum = $A + B + C_{in}$
2. Carry = $BC_{in} + AC_{in} + AB$
3.

14. Give examples for combinational circuits. (A/M 15, N/D 13)
Half Adder, Full adder, Multiplexer, Demultiplexer, encoder, decoder.

15. Construct 4- bit parallel adder/subtractor using full adders and XOR gates. (N/D 14)

16. List out various applications of Multiplexer. (N/D 13)
1.Data routing
2.Parrallel to serial convertion
3.Operating Sequence
4.Logic function generation.

17. Design a single bit magnitude comparator to compare two words A and B.(A/M 11)

a	b	a=b	a>b	a<b
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

a=b: a'b' + ab

a>b: ab'

a<b: a'b

The logic for a=b is also: (a'b + ab')'

18. Write the logic expression for the difference and borrow of a half subtractor.(A/M 11)
Difference= AB'+A'B
Borrow=A'B

19. Define encoder and Decoder?
- A decoder is a multiple - input multiple output logic circuit that converts codedinputs into coded outputs where the input and output codes are different.
- An encoder has 2n input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.

20. Define multiplexer.

Multiplexer is a digital switch. If allows digital information from several sources to be routed onto a single output line.

PART-B

1. Implement the following Boolean function using an 8:1 Multiplexer considering D as the input and A,B,C as selection lines : F (A, B,C,D) = AB'+BD+B'CD'
2. With a neat diagram explain in detail about the working of a 4 bit look ahead carry adder. Also mention its advantage over conventional adder.
3. Design a 4 bit BCD Adder using full adder and explain its structure and compute the circuit to add 1001 and 0101. Write the sum and carry output of the given binary number.
4. Explain the operation and need of priority encoder

5. Design a 5x32 decoder using 3x8 decoder and summerize how many decoders required designing
6. Implement Y = (A+C) (A+D') (A+B+C') using NOR gates only.
7. (i) Why does a good logic designer minimize the use of NOT gates?
   (ii) Show that if all the gates in a two level AND-OR gate networks are replaced by NAND gates the output function does not change.
8. (i) Design and explain 1 of 8 demultiplexer.
   (ii) What is parity checker?
9. Describe the operation of 3-bit magnitude comparator.
10. (i) Design a 4-bit magnitude comparator with 3 outputs : A>B, A=B, A<B.
    (ii) Design a 4 bit binary to gray code converter
11. (i) Implement the following Boolean functions using 8x1 Multiplexers
            F(A,B,C,D) = $\sum$m(1,3,4,11,12,13,14,15)
    (ii) Explain the concept of carry look ahead adder with neat logic diagram.
12. Explain with neat diagram the function of Binary multiplier
    (i) using shift method
    (ii) parallel multiplier.
13. Design a BCD to excess 3 code converter using minimum number of NAND gates.
14. Design a combinational circuit that converts a 4 bit Gray code to a 4 bit binary number.
15. Detail the following (i) BCD adder
                        (ii) Magnitude comparator

PART-C

1. (i) Design a 4 bit decimal adder using 4-bit binary adders.
   (ii) Implement the following Boolean functions using Multiplexers
         F(A,B,C,D) = $\sum$m(0,1,3,4,8,9,15).
2. (i) Design a 4-bit magnitude comparator with three outputs: A>B, A=B and A<B.
   (ii) Construct a 4 bit even parity generator circuit using gate
3. (i) Design 3:8 decoder using basic gates
   (ii) Design a binary to gray code convertor.
4. (i) Design a full subtractor using demultiplexer
   (ii) Explain the working of carry-look ahead adder.
5. Draw the logic diagram of BCD-decimal decoder and explain its operations.
6. Draw the block schematic of magnitude comparator and explain its operations.

UNIT -III SYNCHRONOUS SEQUENTIAL CIRCUITS

PART-A

1. Bring out the difference between synchronous & asynchronous sequential circuits (or) Give the comparison between synchronous & asynchronous sequential circuits?

Synchronous circuits	Asynchronous circuits
Memory elements are clocked flip-flops	Memory elements are either unlocked flip - flops or time delay elements.
Easier to design	More difficult to design

2. A binary ripple counter is required to count upto $16,383_{10}$. How many flip-flops are required? If the clock frequency is 8.192MHz, what is the frequency at the ouput of MSB?

$16,383_{10} = 0b11111111111111$
         0000000000000000
By comparing there are 15 changes the output value is 15.
Clock frequency $= 8.192$ MHZ $= 8192$KHZ
Frequency at output of MSB $= 8192/512 = 16$KHZ

3. Draw the NOR gate latch and write its truth table.
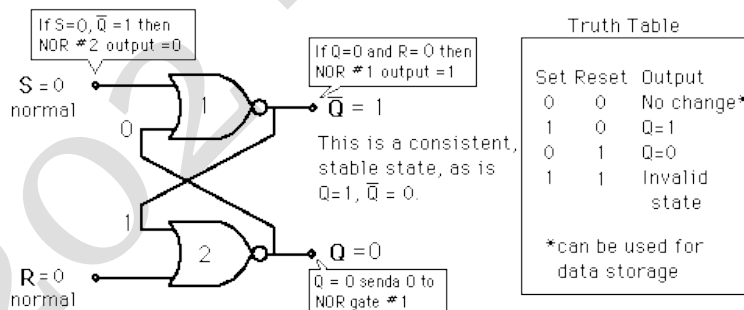
4. Write the difference between synchronous & Asynchronous counters.

Synchronous counter	Asynchronous counter
In this type there is no connection between output of first flip-flop and clock input of the next flip – flop.	In this type of counter flip-flops are connected in such a way that output of 1stflip-flop drives the clock for the next flipflop.
All the flip-flops are clocked simultaneously.	All the flip-flops are Not clocked Simultaneously

5. State the difference between Mealy and Moore model sequential circuits.

Mealy model	Moore model
Its output is a function of present state only.	Its output is a function of present state as well as present input.
An input change does not affect the output.	Input changes may affect the output of the circuit.
Mealy model requires more number of states for implementing same function.	It requires less number of states for implementing same function.

6. Derive the characteristic equation of a D flip flop.

The characteristic equation for D flip-flop is $Q_{n+1} = D$. The output Q_{n+1} is delayed by one clock period. Thus D flip-flop is also known as delay flip-flop.

7. What is the primary disadvantage of asynchronous counter?
- An extra "re-synchronizing" output flip-flop may be required.
- To count a truncated sequence not equal to 2n, extra feedback logic is required.
- Counting a large number of bits, propagation delay by successive stages may become undesirably large.
- This delay gives them the nickname of "Propagation Counters".
- Counting errors occur at high clocking frequencies.
- Synchronous Counters are faster and more reliable as they use the same clock signal for all flip-flops.

8. Define race around condition in flipflop?

In the JK latch, the output is feedback to the input, and therefore changes in the output results change in the input. Due to this in the positive half of the clock pulse if J and K are both high then output toggles continuously. This condition is known as race around condition.

9. Draw D-latch (Transparent latch) with truth table.
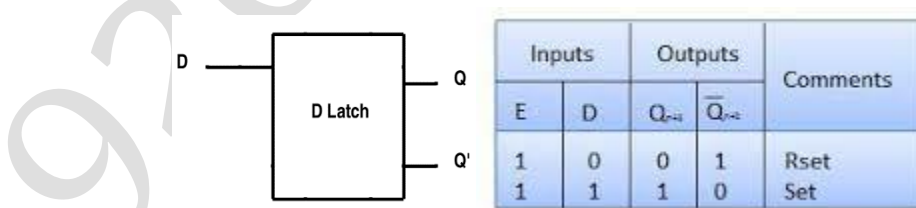
10. What are the classifications of sequential circuits?

The sequential circuits are classified on the basis of timing of their signals into two types. They are, 1) Synchronous sequential circuit.
2) Asynchronous sequential circuit.

11. What is edge-triggered flip-flop?

The problem of race around condition can solved by edge triggering flip flop. The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

12.Draw the truth table of RS flip-flop.

S	R	Q	State
0	0	Previous State	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Forbidden

13. What is the minimum no of flipflop needed to design a counter of modulus 60?

$2^{(n-1)} <= N <= 2^n$
for 60, $2^6 = 64$
So we need 6 flipflops

14. Define Latches.

- It is a memory cell which is capable of storing one bit of information either logic 1 or logic 0.
- This sequential circuit also called a latch since one bit of information can be latched.

15. Define Digital clock.

A digital clock is a type of clock that displays the time digitally (i.e. in numerals or other symbols), as opposed to an analog clock, where the time is indicated by the positions of rotating hands.
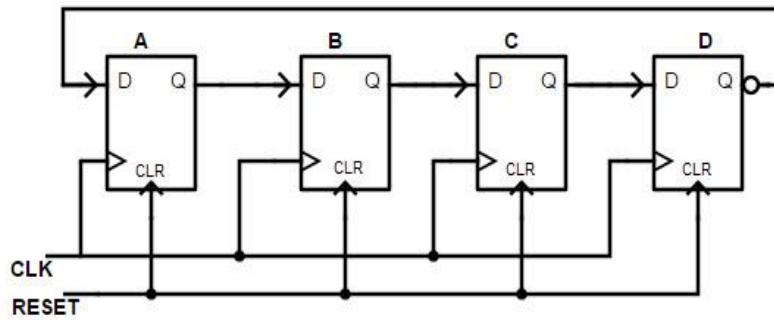
16. Convert D flipflop toT flipflop.

$$D = T'Q + TQ' = T \oplus Q$$

T	Q_n	Q_{n+1}	D	
0	0	0	0	
1	0	1	1	←
1	1	0	0	
0	1	1	1	←

17. Design a 3-bit ring counter and find the mod of the designed counter.

18. Write the characteristic equation of a JK flipflop.

$Q_{(n+1)} = J\,Q_n{}' + K'Q_n$

19. What is meant by flip-flop and types?
　　Latch with the additional control input is called as flipflop. The additional control input is either clock or enable input.
　Types:
- SR flipflop
- JK flipflop
- D flipflop
- T flipflop

20. Define registers.
　　A register is a group of flip-flops flip-flop can store one bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.

PART-B

1. Explain in detail about the ring counter with its logic diagram, state diagram and its sequence table.
2. Discuss in detail about pulse triggered SR flipflop also draw the ouput waveform of this flipflop and explain it with an example.
3. Design a JK counter that goes through states 3,4,6,7 and 3. Is the counter self starting? Modify the circuit such that whenever it goes to an invalid state it comebacks to state 3.
4. A clocked sequential circuit with single input and output x and z respectively, produces an output z = 1, whenever the input x completes the sequence 1011 and overlapping is allowed:
   i) Obtain the state diagram
   ii) Obtain its minimum state table and design the ciruit with D fliplflops.
5. Draw RS flipflop circuit and explain its operation with truth table and suggest how to eliminate the undetermined stage. Write some RS flipflop applications.
6. Discuss the design steps of Asynchronous sequential circuits.
7. Design a 2's complement circuit with shift register and flipflop.The binary number is shifted out from one side and its 2'complement shifted into other side of the shift register.
8. Design and explain the working of a synchronous mod-3 counter.
   Using SR flipflops design a parallel counter which counts in the sequence 000, 111, 101, 110, 010, 000

9. (i) Explain the operation of JK flip-flop with neat diagram.
   (ii) Explain the operation of serial-in-serial-out shift register.
10. Design synchronous MOD-6 counter.
11. Design a 3 bit synchronous counter using D flipflop.
12. (i) Draw and explain the 4-bit SISO, SIPO, PISO and PIPO shift register with its waveforms.
    (ii) Realize D flip-flop using SR flip-flop.
13. (i) Explain the operation of JK flip-flop with neat diagram.
    (ii) Explain the operation of master slave flip flop and show how the race around condition is
       eliminated.
14. Explain the operation of synchronous MOD 6 counter.
15. With a neat sketch describe a 3 bit synchronous up/down counter. Draw the timing
    waveform.

PART-C
1. Design a sequential circuit with two D FFs A and B and one input x. When x = 0, the state of
   the circuit remains the same. When x=1, the circuit gas through the state transitions from 00-
   01-11-10-00-01.
2. Explain the differences between a state table, a characteristics table and an excitation table.

3. Design the sequential circuit specified by the following state diagram using T flip flops.
    Check whether your design is self correctable.
4. Design a sequential circuit that has 3 flip flops A,B and C, one input x and one output y. The
    circuit is to be designed by treating the unused states as don't care conditions. Use JK
    flipflops in the design.
5. Design a moore type sequence detector to detect a serial input sequence of 101.
6.(i) Draw the block diagram of SR-FF and explain (ii) Explain about triggering of flip-flops.

UNIT-IV ASYNCHRONOUS SEQUENTIAL CIRCUITS
PART A

1. What is memory expansion and why is it required?
     Expanded memory, is a technique for utilizing more than 1MB of main memory in DOS -based computers. The limit of 1MB is built into the DOS operating system. The upper 384K is reserved for special purposes, leaving just 640K of conventional memory for programs.

2. A certain memory has a capacity of 32K x 16.How many bits are there in each word? How many words are being stored and how many memory cells does this memory contain?

     1 byte = 8 bits, 1 word = 32 bits,
     Total bits = 32Kx16 = 512000 bits
     640000 words are stored.

3. Distinguish between a flowchart and an ASM chart.

Flowchart	ASM chart
A flowchart is a convenient way to specify the sequence of procedural steps and decision paths for an algorithm.	A special flowchart that has been developed specifically to define digital hardware algorithms is called ASM chart.
A conventional flow chart describes the sequence of procedural steps and decision paths for an algorithm without concern for their time relationship	An ASM chart describes the sequence of as well as the timing relationship between the states of a sequential controller and the events that occur while going from one state to next.

4. What are Hazards and give it types?

       The unwanted switching transients (glitches) that may appear at the output of a circuit is called Hazards.

       Types are 1.Static Hazard

               Static 1 Hazard

               Static 0 Hazard

           2. Dynamic Hazard

5. What is the memory capacity of random access memory if it has 10 bit address lines.

       We have 2^{10} words, each 16 bits wide.

       1B is 8 bits (as usual).

       $2^{10} \times 2 = 2^{11}$ bytes

               $= 2048$ bytes

6. What are the steps for the analysis of asynchronous sequential circuit?

  The procedure to analyze is as follows:

- Determine the next secondary state and output equations from given sequential circuit.
- Construct the state table.
- Construct the transition table.
- Construct output map.

7. What is the significance of state assignment?

- In synchronous circuits-state assignments are made with the objective of circuit reduction
- Asynchronous circuits-its objective is to avoid critical races

8. Define critical race and non critical race

- If the final stable state depends on the order in which the state variable changes, the race condition is harmful and it is called a critical race.
- If the final stable state that the circuit reaches does not depend on the order in which the state variable changes, the race condition is not harmful and it is called a non critical race.
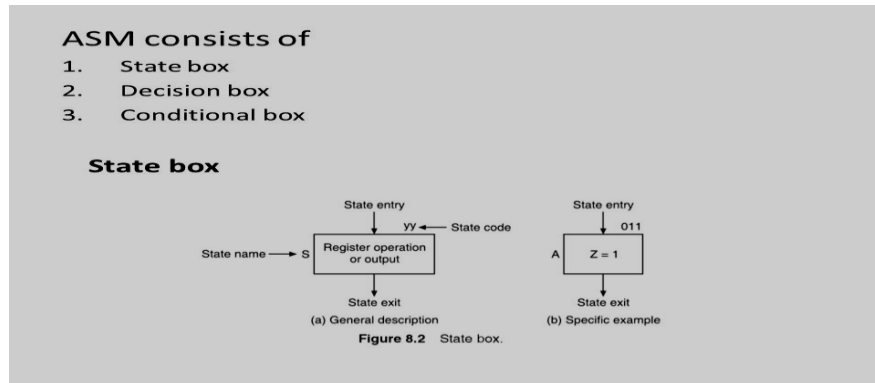
9. Define critical race and give their different methods of critical race free state assignment.

       If the final stable state depends on the order in which the state variable changes, the race condition is harmful and it is called a critical race.

There are 2 methods

1. Shared row state assignment   2.One hot state assignment

10. Draw the general model of ASM.

ASM consists of
1.   State box
2.   Decision box
3.   Conditional box

State box

Figure 8.2   State box.

11. What is static 1 hazard and static 0 hazard?

The unwanted switching transients (glitches) that may appear at the output of a circuit is called Hazards.

- output goes momentarily 0 when it should remain at 1
- output goes momentarily 1 when it should remain at 0

12. Distinguish between a combinational logic circuit and a sequential logic circuit.

Combinational logic	Sequential logic
Combinational logic (sometimes also referred to as time-independent logic) is a type of digital logic which is implemented by Boolean circuits, where the output is a pure function of the present input only	Sequential logic is a type of logic circuit whose output depends not only on the present value of its input signals but on the sequence of past inputs.

13. What is the most important consideration in making state assignments for synchronous network ?

State Reduction & Assignment. Sometimes certain properties of sequential circuits may be used to reduce the number of gates and flip-flops during the design. Sometimes certain properties of sequential circuits may be used to reduce the number of gates and flip-flops during the design.

14. Define ASM chart. List of its three basic elements.

A special flowchart that has been developed specifically to define digital hardware algorithms is called ASM chart. Three basic elements are,

- State Box
- Decision box
- Conditional box

15. What is critical race condition in asynchronous sequential circuit?

If the final stable state depends on the order in which the state variable changes, the race condition is harmful and it is called a critical race.

16. What is state diagram? Give an example

In addition to graphical symbols, tables or equations, flip-flops can also be represented graphically by a state diagram. In this diagram, a state is represented by a circle, and the transition between states is indicated by directed lines (or arcs) connecting the circles. An example of a state diagram is shown in Figure 3 below.
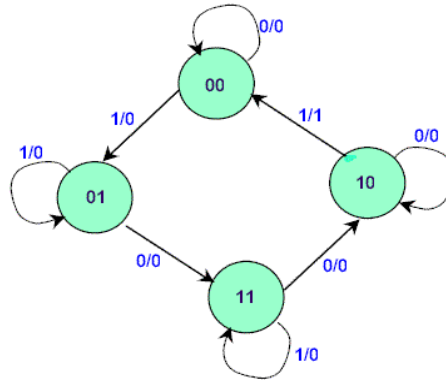
17. Write the VHDL code for half adder.

```
ENTITY  half_adder  is  Half Adder
PORT(a,b:IN BIT; s,c :OUT BIT);
ND  half_adder;
ARCHITECTURE half_adder_beh OF half_adder IS
BEGIN
s <= a XOR b;          -- Implements Sum for Half Adder
c <= a AND b;          -- Implements Carry for Half Adder
END half_adder_beh;
```

18. What is synchronous sequential circuits?
- A Synchronous Sequential circuit is a circuit in which flip-flops are tied to a common clock.
- Memory elements are clocked flip-flops
- Easier to design
- Shift registers and counters are two examples.

19. Differentiate fundamental mode and pulse mode asynchronous sequential circuits?

Fundamental mode	Pulse mode
Input variables changes if the circuit is stable inputs are levels, not pulses only one input can change at a given time.	Inputs are pulses width of pulses are long for circuit to respond to the input pulse width must not be so long that it is still present after the new state is reached.
Delay lines are used as memory elements.	Pulses should not occur simultaneously on two or more input lines.

20. Design a 3 input AND gate using verilog.

```
Module AND_3 (A,B,C,Y);
Input A, B, C;
Output Y;
Assign Y = A&B&C;
End module
```

21. What are the basic building blocks of a algorithmic state machine chart?
   The basic building blocks of algorithmic state machine chart are:
   - State Box
   - Decision box
   - Conditional box

22. What are the two types of asynchronous circuits?
   - 1. Fundamental mode circuits
   - 2. Pulse mode circuits

23. Define state table.
   For the design of sequential counters we have to relate present states and next states. The table, which represents the relationship between present states and next states, is called state table.

24. Under what circumstances asynchronous circuits are preferred?
   Asynchronous circuits can operate faster than synchronous circuits and hence they are preferred when speed is an important criteria.

PART-B

1. (i) Summarize the design procedure for asynchronous sequential circuit.
   (ii) Derive the state table of a serial binary adder.
2. What is the objective of state assignment in asynchronous circuit? Give the hazard free
   realization for the Boolean function $f(A, B, C, D) = M(0, 2, 6, 7, 8, 10, 12)$
3. Explain the steps involved in the design of asynchronous sequential circuit.
4. Design an asynchronous circuit that will output only the second pulse received and ignore any
   other pulse.
5. Design an asynchronous sequential circuit with two inputs X_1 and X_2 and with one output Z.
   When X_1 is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The
   output Z will remain 1 until X_1 returns to 0.
6. Construct the transition table, state table and state diagram for the more sequential circuit.
7. Design a asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1
   when T=1 and c moves from 1 to 0. Otherwise the output is 0.
8. Explain the different methods of race free state assignment.
9. (i) Write the verilog code for full adder and JK FF.
   (ii) Explain the different types of hazards. Design a hazard free circuit for $y = x_1x_2+x_2'x_3$.
10. With ASM chart design a binary multiplier.
11. (i) What is a hazard in an asynchronous sequential circuits? Define static hazard, dynamic
    hazard and essential hazard.

(ii) Write and verify the HDL structural description of the four-bit register with parallel load.
Use a 2x1 multiplexer for the flip-flop inputs. Include an asynchronous clear input

12. Design an asynchronous sequential circuit with inputs A and B and an output Y. Initially and at any time if both the inputs are 0, the output, Y is equal to 0. When A or B becomes 1, Y becomes 1. When the other input also becomes 1, Y becomes 0. The output stays at 0 until circuit goes back to initial state

13. Design a T flip-flop using logic gates. Derive the state table, state diagram, primitive flow table and transition table and merger graph. Draw the logic circuit.

14. Design a asynchronous sequential circuit that has 2 inputs x_1 and x_2 and one output z. When $x_1 = 0$, output is 0. The change in x_2 that occurs while x_1 is 1 will cause output z=1. The output z will remain 1 until x_1 returns to 0.

15. Design a serial binary adder using delay flip-flop.

PART-C

1. List out various problems arises in synchronous circuits. Explain any two problems in detail.
2. Design a hazard free asynchronous circuit that changes state whenever the input goes logic 1 to logic 0.
3. Define races and hazards in detail
4. Design a serial binary adder using JK flip-flop.
5. Explain the steps involved in the design of synchronous sequential circuit.

UNIT-V LOGIC FAMILIES AND PROGRAMMABLE LOGIC DEVICES

PART-A
1. Write the types of programmable logic devices.
- Programmable Logic Array (PLA)
- Programmable Array Logic (PAL)
- Generic Logic Array (GLA)
- Complex Programmable Logic Device (CPLD)
- Field Programmable Gate Array (FPGA)

2. How does ROM retain information?
ROM is used to store the binary code for the sequence of instructions that the computer to carry out and data such as look up tables. This is because this type of information does not chang

3. Differentiate between PAL and PLA.

S.no	PLA	PAL
1.	Both AND and OR arrays are programmable.	OR array is fixed and AND array is programmable.
2.	Costliest and complex than PAL and PROMs.	Cheaper and simpler.
3.	AND array can be programmed to get desired minterms.	AND array can be programmed to get desired minterms.
4.	Any Boolean functions in SOP form can be implemented using PLA.	Any Boolean functions in SOP form can be implemented using PLA.

4. Briefly explain EEPROM.

EEPROM(Electrically Erasable Programmable Read Only Memory) EEPROM also use MOS circuitry. Data is stored as charge or no charge on an insulated layer or an insulated floating gate in the device. EEPROM allows selective erasing at the register level rather than erasing all the information since the information can be changed by using electrical signals.

5. What is programmable logic array? How it differs from ROM?

A programmable logic array (PLA) is a kind of programmable logic device used to implement combinational logic circuits. ... It has 2^N AND Gates for N input variables and for M outputs from PLA, there should be M OR Gates, each with programmableinputs from all of the AND gates.

6. How Bipolar RAM cell is differ from MOSFET RAM cell.

In Bipolar RAM cell the memory cell is implemented by TTL. It stores 1 bit of information. It is nothing but a flipflop.

In MOSFET RAM cell enhancement mode MOSFET transistors are used to make this RAM cell. It is very similar to TTL cell.

7. What is Read and Write operation?

- The Write operation stores data into a specified address into the memory and the
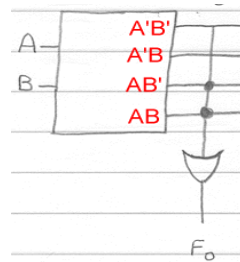- Read operation takes data out of a specified address in the memory.

8. What is the basic difference between the RAM & ROM circuitry ?

RAM	Differences	ROM
❖ stores during and after processing	Data and Program	❖ stored by manufacturer
❖ stores information temporarily	Content	❖ stores information permanently
❖ very fast but uses a lot of power	Processing Time	❖ fast but uses very little power
❖ volatility	Volatile	❖ non-volatile

9. Compare static and dynamic RAM cell.

S.No	SRAM	DRAM
1.	Stores data till the power is supplied.	Stores data only for few milliseconds even when power is supplied.
2.	Uses an array of 6 transistors for each memory cell	Uses a single transistor and capacitor for each memory cell.
3.	Does not refreshes the memory cell	Needs to refresh the memory cell after each reading of the capacitor.
4.	Data access is faster	Data access is slower

10. Y=AB'+AB Implement using ROM.

11. Compare and contrast EEPROM and flash memory.

| EEPROM	Flash memory
EEPROM(Electrically Erasable Programmable Read Only Memory) EEPROM also use MOS circuitry. Data is stored as charge or no charge on an insulated layer or an insulated floating gate in the device. EEPROM allows selective erasing at the register level rather than erasing all the information since the information can be changed by using electrical signals.	They are high density read/write memories that are non-volatile, which means datacan be stored indefinitely with out power. The traditional memory technologies such as ROM, PROM, EEPROM individually exhibits one of these characteristics, but no single technology has all of them except the flash memory.

12. What is field programmable logic array?

The second type of PLA is called a field programmable logic array. The user by means of certain recommended procedures can program the PLA.

13. List the advantages of PLDs.
- Lower Power Requirements
- Less Costly Assembly Processes
- Higher Reliability
- Availability Of Design Software
- Less Board Space, Faster

14. Draw the structure of a static RAM cell.
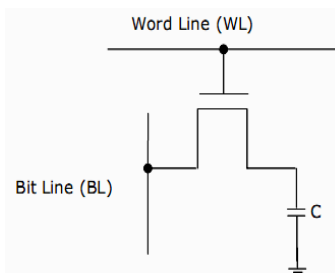
15. What is volatile and Non volatile memory?

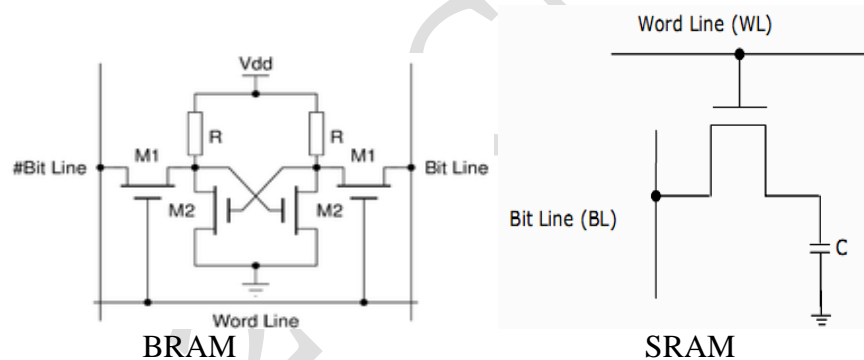| Volatile memory	Non volatile memory
Any type of memory requires some power to store the binary information. All information's are lost when the power is removed.	The contents of memory is not lost even when the power is removed from the memory.

16. List the advantages of RAM
- Fast access of data.
- High Ram capacity increase the speed of the system
- It helps fast start up and shut down of the computer.
- It is a volatile memory of the system.

17. What are the different types of programmable logic devices?
1. Read only memory
2. Programmable logic Array
3. Programmable Array Logic

18. Draw the logic diagram of SRAM and BRAM cell.
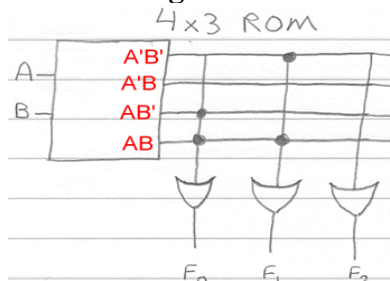

BRAM

SRAM

19. How the memories are classified?
Memories are classified into
- Volatile memory
- Non-volatile memory

20. Implement the Exclusive Or Function Using ROM.

21. Define Static RAM and dynamic RAM.
- Static RAM use flip flops as storage elements and therefore store data indefinitely as long as dc power is applied.
- Dynamic RAMs use capacitors as storage elements and cannot retain data very long without capacitors being recharged by a process called refreshing.

22. What are the types of ROM?
    1.PROM
    2.EPROM
    3.EEPROM

23. Define bit, byte and word.
    The smallest unit of binary data is bit. Data are handled in a 8 bit unit called byte. A complete unit of information is called a word which consists of one or more bytes.

24. Why RAMs are called as Volatile?
    RAMs are called as Volatile memories because RAMs lose stored data when the power is turned OFF.

25. Define Cache memory.
    It is a relatively small, high-speed memory that can store the most recently used instructions or data from larger but slower main memory.

26. Define address of a memory and Capacity of a memory.
- The location of a unit of data in a memory is called address.
- It is the total number of data units that can be stored.

PART-B
1. Write the program table to implement a BCD to excess 3 code conversion using a PLA.
2. Explain in detail about the working of bipolar SRAM cell and single transistor DRAM cell with neat sketches.
3. Explain the TTL circuit with open collector output.
4. (i) Compare static RAM and Dynamic Ram
  (ii) Implement the switching functions
   $z1 = ab'd'e + a'b'c'e'+ bc+de$
   $z2 = a'c'e$
   $z3 = bc+de+c'd'e'+bd$ and $z4 = a'c'e+ce$ using a 5*8*4 PLA.
5. (i) Distinguish between Boolean addition and binary addition.
  (ii) Design a combinational circuit using a ROM that accepts a 3 bit number and generates an output binary number equal to the square of the given number.
6. Differentiate static and dynamic RAM. Draw the circuits of one cell of each and explain its working principle.
7. Write short notes on (i) PAL (ii) FPGA.
8. Implement the following function using PLA.
    $F1(x,y,z) = \sum m(1,2,4,6)$
    $F2(x,y,z) = \sum m(0,1,6,7)$
    $F3(x,y,z) = \sum m(2,6)$
9. (i) Explain memory READ and WRITE operation with neat timing diagram.

(ii) Explain the organization of ROM with relevant diagrams.

10. Give an account for classification of memories.

11. Explain the structure of PAL and PLA. How a combinational logic function is implemented in PAL and PLA? Explain with an example for each.

12. (i) Write short notes on EAPROM and static RAM cell using MOSFET.

(ii) Using eight 64x8 ROM chips with an enable input and a decoder, construct a 512 x 8 ROM.

13. (i) Implement a 3 bit up/down counter using PAL devices.

(ii) Implement binary to Gray code converter using PROM devices.

14. Discuss in detail about field programmable gate array

15. Discuss in detail about programmable array logic

PART-C

1. Write the program table to implement a BCD to gray code conversion using a PLA

2. Explain static RAM cell using MOSFET

3. Illustrate the circuit operation and characteristics of TTL NAND logic gate in detail

4. Define the working of PLA

5. Summarize the design procedure of synchronous sequential circuit

Faculty Incharge   **Head of the Department**

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HoD Remarks: